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09/872,600	06/01/2001	Kevin B. Leigh	COMP:0213	2616

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EXAMINER	
HUYNH, KIM T	

ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 08/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/872,600	LEIGH ET AL.	
	Examiner	Art Unit	
	Kim T. Huynh	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-55* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-55* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *6/1/01* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-10, 12-21, 23-31, 35-41, 43-50, 52-55 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vivio (US Patent 5,706,447) in view of Alexandria (US Patent 6,701,402)

As per claims 1,13, Vivio discloses a method of switching control of a bus in a processor-based device, the method comprising the acts of:

- Electrically coupling a first bus controller to the bus; (col.4, lines 18-36)
- Generating a detection signal indicative of coupling of a second bus controller to the bus; and (col.4, lines 18-12)

Vivo discloses all the limitations as above except automatically isolating the first bus controller from the bus in response to the detection signal. However, Alexander discloses when controller is given master access to bus, controller is the only master communicating with the disk controller, other masters connected to bus are not communicate with disk controller until controller relinquishes master access to bus. (col.3, lines 7-13)

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Alexander's teaching into Vivo's

system so as to facilitate the use of preexisting controller in a host for a peripheral device connected to the host. (col.1, lines 44-46)

As per claim 2, Vivio discloses the method comprising the act of terminating the first bus controller. (col.4, lines 18-62)

As per claim 3, Vivio discloses wherein the first bus controller is terminated response to detection of the detection signal. (col.4, lines 18-36)

As per claim 4, Vivio discloses wherein the bus comprises a plurality of traces disposed on a substrate, wherein the first bus controller is electrically coupled to a first segment of the plurality of traces, and wherein the second bus controller is electrically coupled to a second segment of the plurality of traces. (col.7, lines 5-48), wherein substrate equipped within connector)

As per claim 5, Vivio discloses the method comprising the act of terminating the second segment of the plurality of traces. (col.7, lines 5-48)

As per claim 6, Vivio discloses the method comprising the act of electrically removing terminating of the second segment of the plurality of traces in response to detection of the second bus controller. (col.7, lines 5-48)

As per claim 7, Vivio discloses wherein the first bus controller is disposed on a first substrate, and the second controller is disposed on a second substrate, the second substrate being coupled to the first substrate, and wherein the act of generating a detection signal comprises the act of transmitting the detection signal from the second substrate to the first substrate. (col.7, lines 5-56), fig.3, (col.4, lines 18-62)

As per claim 8, Vivio discloses wherein the first substrate comprises an expansion port, and a first end of the cable is connected to the expansion port. (col.6, lines 36-52), (claim 1, col.9, lines 35-48)

As per claims 9, 31,50, discloses wherein the bus comprises a SCSI bus.

As per claim 10, Vivio discloses wherein the first substrate and the second substrate each comprise a printed circuit board. (col.7, lines 5-56), fig.3, (col.4, lines 18-62)

As per claim 12, Vivio discloses wherein the act of electrically coupling comprises the act of coupling the first bus controller to the bus using a switch. (claim 1, col.9, lines 53-62)

As per claim 14, Vivio discloses wherein the act of detecting the presence of the second bus controller comprises the act of generating a detect signal when the second bus controller is electrically coupled to the bus. (col.4, lines 18-62)

As per claim 15, Vivio discloses wherein the act of automatically switching control of the bus comprises the acts of:

- Isolating the first bus controller from the bus; and (col.4, lines 18-62)
- Terminating the isolated first bus controller. (col.4, lines 18-62)

As per claims 16, 46, Vivio discloses the method comprising the act of terminating the bus proximate the first bus controller. (col.9, lines 42-44)

As per claim 17, Vivio discloses wherein the bus is terminated proximate the first bus controller in response to detecting the presence of the second bus controller. (col.4, lines 18-62)

As per claim 18, Vivio discloses wherein the second bus controller is disposed on a second substrate coupled to the first substrate. (col.7, lines 5-48), wherein substrate equipped within connector)

As per claim 19, Vivio discloses wherein the first substrate comprises an expansion port, and the method comprises the act of terminating the bus proximate the expansion port. (col.9, lines 42-44)

As per claim 20, Vivio discloses the method comprising the act of removing termination of the bus proximate expansion port in response to detecting the presence of the second bus controller. (col.4, lines 18-62)

As per claim 21, Vivio discloses the method of switching control of a bus in a low profile server, the low profile server comprising a first bus controller, a bus, and an isolation device, wherein the first bus controller is configured to control the bus, and wherein the isolation device is configured to isolate first bus controller from the bus(col.4, lines 18-62). Vivo discloses all the limitations as above except the method comprising the act of connecting a second bus controller to the bus to cause the isolation device to isolate the first bus controller from the bus. However, Alexander discloses when controller is given master access to bus, controller is the only master communicating with the disk controller, other masters connected to bus are not communicate with disk controller until controller relinquishes master access to bus. (col.3, lines 7-13)

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Alexander's teaching into Vivo's

system so as to facilitate the use of preexisting controller in a host for a peripheral device connected to the host. (col.1, lines 44-46)

As per claims 23, 35, Vivio discloses a processor-based device, comprising:

- A processor; (fgi.1, 122)
- A memory coupled to the processor; and (fig.1, 124)
- A first substrate, comprising:
    - A bus disposed on the first substrate; (col.7, lines 5-48), wherein substrate equipped within connectors)
    - A first bus controller disposed on the first substrate, the first bus controller being coupled to the processor and the bus; and (col.4, lines 18-62)
    - An isolation device disposed on the first substrate, the isolation device being configured to couple the first bus controller to the bus,

Vivo discloses all the limitations as above except automatically isolating the first bus controller from the bus in response to the detection signal. However, Vivo discloses all the limitations as above except automatically isolating the first bus controller from the bus in response to the detection signal. However, Alexander discloses when controller is given master access to bus, controller is the only master communicating with the disk controller, other masters connected to bus are not communicate with disk controller until controller relinquishes master access to bus. (col.3, lines 7-13)

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Alexander's teaching into Vivo's system so as to facilitate the use of preexisting controller in a host for a peripheral device connected to the host. (col.1, lines 44-46)

As per claim 24, Vivio discloses the device comprising an expansion port disposed on the first substrate and coupled to the bus, wherein the expansion port is connectable to a second substrate, and wherein the second bus controller is disposed on the second substrate. (col.7, lines 5-48)

As per claim 25, Vivio discloses wherein the second bus controller is disposed on a second substrate, and the device comprises a cable having a first end and a second end, the first end being connectable to the first substrate, and the second end being connectable to the second substrate. (col.7, lines 5-48)

As per claim 26, Vivio discloses the device comprising a termination device disposed on the first substrate, the termination device being configured to terminate the bus proximate the expansion port when the second bus controller is not coupled to the bus. (col.9, lines 42-44), (col.7, lines 5-48)

As per claim 27, Vivio discloses the device comprising a termination device disposed on the first substrate, the termination device being configured to terminate the bus proximate the first bus controller in response to detection of the second bus controller. (col.4, lines 3-62)

As per claims 28, 39, Vivio discloses wherein the isolation device comprises an electronic switch. (claim 1, col.9, lines 53-62)

As per claims 29, 40, Vivio discloses wherein the electronic switch comprises a transistor. (fig.3, col.7, lines 5-48)

As per claim 30, Vivio discloses wherein the processor and the memory are disposed on the first substrate. (Fig.5, 120 i/o)

As per claim 36, Vivio discloses the board comprising a termination device disposed on the substrate and configured to terminate the first bus controller in response to detection of the second bus controller coupled to the bus. (col.4, lines 18-62)

As per claim 37, Vivio discloses the board comprising an expansion port disposed on the substrate and coupled to the bus, wherein the second bus controller is coupled to the bus via the expansion port. (col.7, lines 5-48)

As per claim 38, Vivio discloses the board comprising a termination device disposed on the substrate and configured to terminate the bus proximate the expansion port when the second bus controller is not coupled to the bus via the expansion port. (col.7, lines 5-48)

As per claim 41, Vivio discloses the printed circuited board comprising:

- A memory disposed on the substrate; and (fig.5, 120 I/O)
- A processor disposed on the substrate, the processor being coupled to the memory and to the first bus controller.(fig.5, 120 I/O)

As per claim 44, Vivio discloses a method of manufacturing a device for switching control of a bus in a processor-based device, the method comprising the acts of:

- Providing a bus disposed on a substrate; (fig.5, connector 210, 510)
- Connecting an expansion port to the bus, the expansion port being configured for connection to a second bus controller; (col.7, lines 5-48)
- Disposing an isolation device on the substrate, the isolation device being connected to the bus; and (col.7, lines 5-48)
- Disposing a first bus controller on the substrate, the first bus controller being connected the isolation device (col.4, lines 18-62), (col.7, lines 5-48)

Vivo discloses all the limitations as above except the isolation device being configured to isolate the first bus controller from the bus when a second bus controller is connected to the expansion port. However, Alexander discloses when controller is given master access to bus, controller is the only master communicating with the disk controller, other masters connected to bus are not communicate with disk controller until controller relinquishes master access to bus. (col.3, lines 7-13)

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Alexander's teaching into Vivo's system so as to facilitate the use of preexisting controller in a host for a peripheral device connected to the host. (col.1, lines 44-46)

As per claim 45, Vivio discloses the method comprising the act of disposing a termination device on the substrate, the termination device being connected to the bus. (col.4, lines 18-62)

As per claim 47, Vivio discloses the method wherein the termination device is configured to terminate the first bus controller when the second bus controller is connected to the expansion port. (col.7, lines 5-48)

As per claim 48, Vivio discloses wherein the termination device is connected to the bus proximate the expansion port. (col.9, lines 42-44)

As per claim 49, Vivio discloses wherein the termination device is configured to terminate the bus proximate the expansion port when the second bus controller is not connected to the expansion port. (col.9, lines 42-44) (col.7, lines 5-48)

As per claim 52, Vivio discloses a method of manufacturing an expansion card connectable to system controller board having a system bus controller configured to control the bus, and having an isolation device configured to isolate the system bus controller from the bus in response to a detect signal, the method comprising the acts of:

- Disposing an expansion us controller on a substrate, the expansion bus controller being configured to control a bus; (col.4, lines 18-62)
- Disposing a detect signal generator on the substrate; (col.7, lines 5-48)
- Connecting the detect signal generator to the first expansion connector; and (col.7, lines 5-48)
- Disposing a first expansion connector on the substrate, the first expansion connector connected to the expansion bus controller and the detect signal generator, (col.7, lines 5-48)

- Wherein the first expansion connector is configured to couple with a cable, the cable having a first end connectable to the first expansion connector and a second end connectable to a system controller board, and (fig.3, and fig.5), (col.7, lines 5-48)
- Wherein the detect signal generator is configured to generate a detect signal detectable at the second end of the cable when the expansion board is connected to the system board via the cable. (fig.3, and fig.5), (col.7, lines 5-48)

Vivo discloses all the limitations as above except wherein the isolation device is configured to isolate the system bus controller from the bus in response to the detect signal. However, Alexander discloses when controller is given master access to bus, controller is the only master communicating with the disk controller, other masters connected to bus are not communicate with disk controller until controller relinquishes master access to bus. (col.3, lines 7-13)

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Alexander's teaching into Vivo's system so as to facilitate the use of preexisting controller in a host for a peripheral device connected to the host. (col.1, lines 44-46)

As per claim 53, Vivio discloses a method of switching between a first device and a second device connectable to a communications medium in a processor-based device, the method comprising the acts of:

- Electrically coupling a first device to the communications medium; (col.4, lines 58-62)
- Generating a detection signal indicative of coupling of a second device to the communications medium; and (col.4, lines 18-62)

Vivo discloses all the limitations as above except automatically isolating the first device from the communications medium in response to the detection signal. However, Alexander discloses when controller is given master access to bus, controller is the only master communicating with the disk controller, other masters connected to bus are not communicate with disk controller until controller relinquishes master access to bus. (col.3, lines 7-13)

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Alexander's teaching into Vivo's system so as to facilitate the use of preexisting controller in a host for a peripheral device connected to the host. (col.1, lines 44-46)

As per claim 54, Vivio discloses wherein the communications medium comprises a point-to-point interconnect. (col.7, lines 5-48)

As per claim 55, Vivio discloses wherein the communications medium comprises shared bus. (fig.5, bus 120)

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 11,22, 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vivio (US Patent 5,706,447) in view of Alexandria (US Patent 6,701,402), and further in view of Applicant Admitted Prior Art

As per claims 11 and 34, Vivio discloses all the limitations as above except a low profile server. However Applicant admitted prior art discloses designs of low profiles servers which have a reduced height between the base and top of the chassis. (page 2, lines 23-24)

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate AAPA's teaching into Yanagisawa's method so as to reduce the height.

As per claim 22, Vivio discloses wherein the first bus controller is disposed on a first substrate, and wherein the second bus controller is disposed on a second substrate, and the act of connecting the second bus controller to the bus comprises the acts of:

- Disposing a cable, the cable comprising a first end and a second end; (col.7, lines 5-48, fig.4)
- Connecting the first end of the cable to the first substrate; and (col.7, lines 5-48, switch 222)
- Connecting the second end of the cable to the second substrate. (col.7, lines 4-48, fig.5)

Yanagisawa discloses all the limitations as above except a low profile server. However Applicant admitted prior art discloses designs of low profiles servers which have a reduced height between the base and top of the chassis. (page 2, lines 23-24)

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate AAPA's teaching into Yanagisawa's method so as to reduce the height.

5. Claims 32-34, 42, 51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vivio (US Patent 5,706,447) in view of Alexandria (US Patent 6,701,402) and further in view of Gasparik et al. (US Patent 6,072,943)

Vivio discloses all the limitations as above except a SCSI device connectable/operatable to the SCSI bus. However, Gasparik discloses the SCSI bus is designed to connect independent devices, such as a SCSI bus 20 couples first SCSI device 12 to SCSI 14 which provides a communication path between the device 12 and 14. (col.3, lines 52-67)

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Gasparik's teaching into Vivio's system so as to provide each SCSI device with termination capabilities. (col.2, lines 11-15)

Response to Amendment

6. Applicant's appeal brief filed on 5/31/05 have been fully considered but are moot in view of the new ground(s) of rejection.

Conclusion

7. *Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kim Huynh whose telephone number is (571)272-3635 or via e-mail addressed to [kim.huynh3@uspto.gov]. The examiner can normally be reached on M-F 9.00AM- 6:00PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached at (571)272-3676 or via e-mail addressed to [rehana.perveen@uspto.gov].*

The fax phone numbers for the organization where this application or proceeding is assigned are (571)273-8300 for regular communications and After Final communications. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571)272-2100.

PAUL R. MYERS
PRIMARY EXAMINER

Kim Huynh

August 8, 2005